Design Guidelines for RT7302 and RT7304 PSR LED Driver

Abstract

RT7302 and RT7304 are constant current LED drivers with active power factor correction (PFC). They support high power factor across a wide range of line voltages, and drive the converter in the quasi-resonant (QR) mode to achieve higher efficiency. By using primary side regulation (PSR), RT7302/RT7304 control the output current accurately without the need of a shunt regulator or opto-coupler at the secondary side, reducing the external component count, the cost, and the size of the driver board.

This application note presents a step by step design guideline for an isolated single stage constant current LED driver with PFC using the RT7302. The guideline can also be applied to RT7304.
The design example in this application note describes an 18W LED driver with slim form-factor, suitable for T8 LED tube applications, but the same design can also be used in LED bulb or other form factor applications.

Contents

1. Introduction

RT7302 and RT7304 are constant current LED drivers with active power factor correction (PFC). They support high power factor across a wide range of line voltages, and drive the converter in the quasi-resonant (QR) mode to achieve higher efficiency. By using primary side regulation (PSR), RT7302/RT7304 control the output current accurately without a shunt regulator or opto-coupler at the secondary side, reducing the external component count, the cost, and the size of the LED driver board.

RT7304 embeds comprehensive protection functions for robust designs, including LED open circuit protection, LED short circuit protection, output diode short circuit protection, VDD under voltage lockout (UVLO), VDD over-voltage protection (VDD OVP), over-temperature protection (OTP), and cycle-by-cycle current limitation. RT7304 is available in a cost effective SOT-23-6 package.

RT7302 has the same basic functionality as RT7304, but integrates more features, including fast startup via high voltage pin, PWM dimming, and input voltage feed-forward compensation. RT7302 is available with SOP-8 package.

This application note presents a step by step design guideline for an isolated single stage constant current LED driver with PFC using the RT7302. The design guideline can also be applied to RT7304.

The design example in this application note is an 18W LED driver with slim form-factor, suitable for T8 LED tube applications.

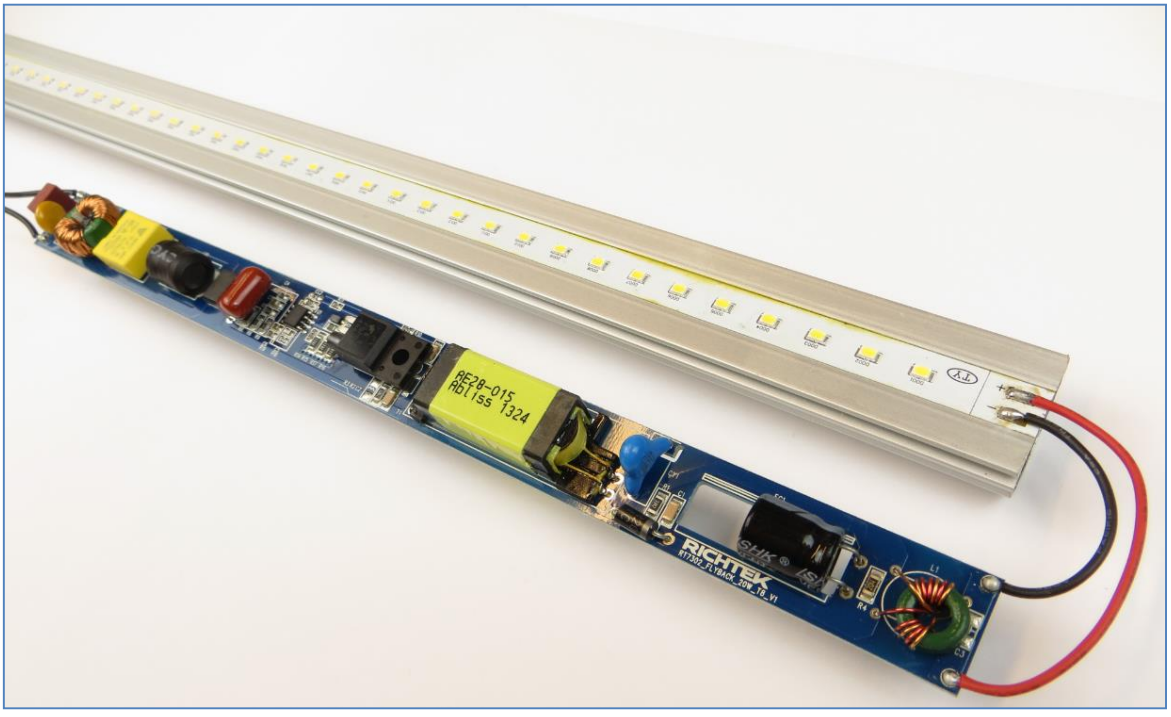


Figure 1. Picture of the 18W evaluation board with a typical T8 LED assembly

2. RT7302 Basic Operation

Figure 2 shows RT7302 in a typical flyback converter topology with input voltage (V_{in}).

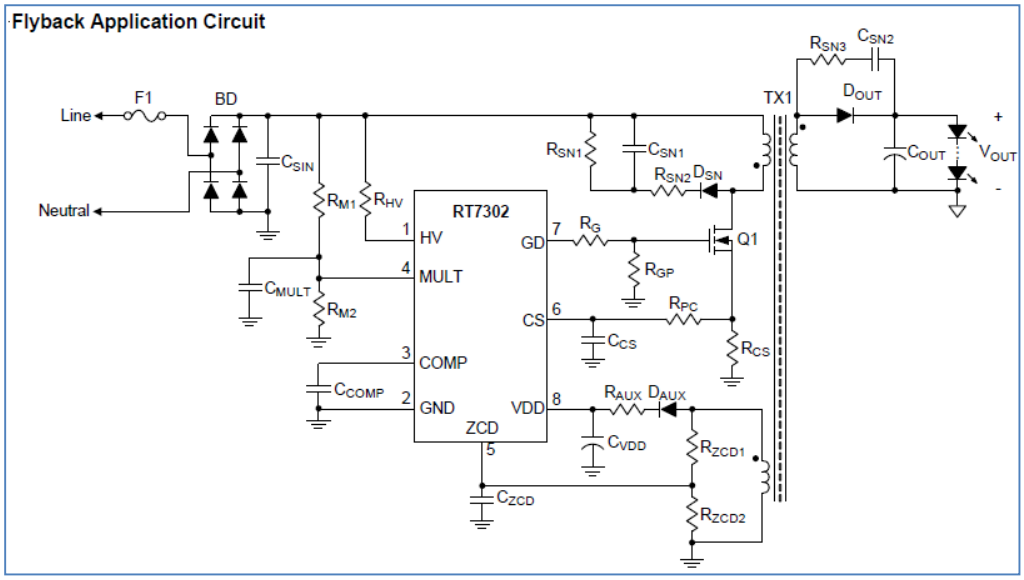


Figure 2

When main switch Q1 is turned on with a fixed on-time t_{on}, the peak current I_{L_pk} of the magnetic inductor L_m can be calculated by the following equation:

$$I_{L\_pk} = \frac{V_{in}}{L_m} \times t_{on}$$

If the input voltage is the output voltage of the full-bridge rectifier with sinusoidal input voltage $V_{in\_pk} \cdot \sin(\theta)$, the inductor peak current I_{L_pk} can be expressed as the following equation:

$$I_{L\_pk} = \frac{V_{in\_pk} \cdot |\sin(\theta)| \times t_{on}}{L_m}$$

When the converter operates in critical-conduction mode (CRM) with constant on-time control, the envelope of the peak inductor current will follow the input voltage waveform in-phase. Thus, high power factor can be achieved. The minimum on time is set by the upper divider resistor of the ZCD network R_{ZCD1}.

Quasi resonant switching is achieved by sensing the auxiliary winding zero current condition and a smart internal valley detection circuit. Switch-on of the MOSFET will always happen at a valley of the resonant voltage, thereby reducing switching losses and EMI. The ZCD pin is also used to sense output OVP condition, set by R_{ZCD2}.

The primary peak current is sensed by measuring the voltage across the MOSFET source resistor via the CS pin. An internal leading edge blanking circuit removes any spikes from this signal. A current variation due to a propagation delay is compensated by the CS pin internal current source and the external series resistor R_{PC}.

The MULT pin is used for sensing the input peak voltage, and controls the ramp for T-on generation. The line voltage sense is used as feed-forward to adjust the ramp for constant COMP voltage over line voltage. This improves the regulation, eases compensation and achieves accurate maximum power limit over the full mains range. This is especially important for full range LED driver designs.

RT7302 HV pin will quickly charge the capacitor connected to the VDD pin during start-up. After start-up, the HV pin is disconnected, and the VDD is supplied by the auxiliary winding. This method ensures fast start-up without extra power dissipation in the bleeder resistor during normal operation.

Design Procedure:

The basic design sequence is as following:

Define Input and output conditions → Calculate input power → Transformer design, Calculate N ratio, Primary inductance, Primary and secondary winding turns → Current sense resistor (R_{CS}), bridge rectifier, MOSFET parameters, Output diode parameters → Minimum ton setting (R_{ZCD1}) → OVP setting (R_{ZCD2}) → Propagation delay setting (R_{PC}) → Feed-forward compensation (R_{M1}, R_{M2})

The RT7302 design tool can be used to quickly determine the component values. Chapter 3 contains a detailed step by step design description for the 18W reference design.

3. Design of an 18W LED Driver for T8 Applications

The LED driver example for this section is the 18W T8 LED driver evaluation board, see Figure 3.

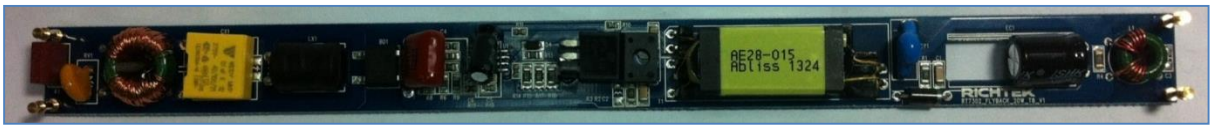


Figure 3. The board measures 230x18x10mm and will fit in most narrow tube T8 housing behind the LED board.

Requirement specification for this design:

- Input range: 90V ~ 264V_{ac}
- LED load: 45V / 400mA
- Efficiency >85% at 120V / 230V_{ac}
- PF: > 0.95 and THDi < 15% (meet IEC61000-3-2 class C & D)

Step 1. Input and Output Conditions

The input and output conditions are listed as follows:

maximum AC input voltage V_{ac_max}, 264V_{ac}

minimum AC input voltage V_{ac_min}, 90V_{ac}

line frequency f_{line}, 50Hz / 60Hz

average output current I_O, 400mA

minimum average output voltage V_{o_min}, 43V

maximum average output voltage V_{o_max}, 47V

LED string is using 14 high power LEDs with total dynamic resistance of 14Ω

Estimated maximum average input power $P_{in\_max\_est}$ can be expressed as:

$$P_{In\_max\_est} = \frac{V_{o\_max} \cdot I_o}{\eta}$$ where η is the estimated efficiency.

The efficiency is estimated at 85%, the input power will become : 47*0.4/0.85 = 22.12W.

Estimated peak current transfer ratio of the transformer (CTR_{TX1}) can be expressed as

$$CTR_{TX1} = \frac{I_{SEC\_PK}}{I_{PRI\_PK}} \times \frac{N_S}{N_P}$$

where I_{SEC_pk} is the peak current of secondary side, I_{PRI_pk} is the peak current of the primary side, N_S is the turn's number of the secondary winding, and N_P is the turn's number of the primary winding. CTR_{TX1} can be estimated to be 0.9.

The reflected output voltage Vro can be express as

$$v_{ro} = \frac{N_P}{N_S} \cdot \left(V_{o\_max} + V_f \right)$$

where V_f is the forward voltage of output diode. V_{ro} is recommended to be within 95 ~125V.
In the example: Set V_{ro} = 125V.

Min. VDD supply voltage at max. output voltage $V_{DD\_Vomax\_min}$ can be derived as

$$V_{DD\_Vomax\_min} = \frac{V_{o\_max}}{V_{o\_min}} \cdot V_{TH\_OFF\_max} \cdot 130\%$$

where V_{TH_OFF} is the falling under voltage lockout (UVLO) threshold voltage of the controller.

VDD supply voltage at max. output voltage V_{DD_max} must be within $V_{DD\_Vomax\_min}$ ~ $V_{DD\_OVP\_min}$.

In the example:
V_{O_max} = 47V, V_{O_min} = 43V, $V_{TH\_OFF\_max}$ = 10V, $V_{DD\_Vomax\_min}$= 14.2V
Set V_{DD_max} = 20V.

Output Capacitor C_{OUT} Calculation:

The output capacitor value will determine the amount of voltage ripple on the LED string. This voltage ripple, together with the dynamic resistance of the LED string will determine the current ripple through the LED string and this will cause 100Hz or 120Hz light flicker.

In this example the maximum allowed LED current ripple amplitude is set at 340mApp for a ripple percentage of 42%. The LED string uses 14 LEDs and has total dynamic resistance of 14Ω: V_{OUT} ripple = 0.34A*14 Ω = 4.76Vpp. The transformer secondary winding current can estimated having a low frequency ripple of double the line frequency and low frequency peak to peak amplitude of double the average output current. The output capacitor value can now be calculated:

$$C_{OUT} = \frac{I_{OUT\_PP}}{V_{OUT\_PP} \cdot 2 \cdot \pi \cdot f}$$

where I_{OUT_PP} is 2x the average LED current, and V_{OUT_PP} is the allowed AC output voltage ripple and f is double line frequency. Calculating for 50Hz line frequency: C_{OUT} = 2*0.4/(4.76*2*π*100) = 267μF. For less LED current ripple, the C_{OUT} value needs to be increased. But when LED strings with higher dynamic resistance are used, the C_{OUT} value can be reduced.

Step 2. Transformer Design

Ideal turn's ratio of primary to secondary windings can be expressed as

$$\frac{N_P}{N_S}=\frac{V_{ro}}{V_{o\_max}+V_f}$$

In the example:

V_{ro} = 125V, V_{O_max} = 47V, V_f = 0.7V, N_P/N_S= 2.62

Ideal turn's ratio of secondary to auxiliary windings can be expressed as

$$\frac{N_S}{N_A}=\frac{V_{o\_max}}{V_{DD\_max}}$$

In the example:

V_{O_max} = 47V, V_{DD_max} = 20V, N_S/N_A = 2.35

The maximum on time of the MOSFET ton_max can be expressed

$$t_{on\_max}=D_{on\_max}\cdot\frac{1}{f_{s\_min}}$$

in which f_{s_min} is the minimum switching frequency.

The duty ratio of the MOSFET D_{on} can be expressed

$$D_{on\_max}=\frac{V_{ro}}{V_{ro}+V_{ac\_min\_pk}}$$

The primary-side inductance Lm can be derived as

$$L_m=\frac{t_{on}}{2I_o}\cdot\frac{N_P}{N_S}\cdot CTR_{TX1}\frac{\int_0^{\frac{1}{2f_{line}}}\frac{V_{ac}(t)^2}{V_{ro}+V_{ac}(t)}dt}{\frac{1}{2f_{line}}}$$

Thus, L_m can be obtained after the minimum switching frequency f_{s_min} is determined.

In the example:

Set f_{s_min} = 54kHz,

V_{ro} = 125V, $V_{ac\_min\_pk}$ = 127V,

Obtain t_{on_max} = 8.68μs and L_m = 899μH

The minimum number of turns for the transformer primary side to avoid the core saturation is given by:

$$N_{P\_min} > \frac{I_{P\_pk} \cdot L_m}{B_{max} \cdot A_e}$$

where A_e is the cross-sectional area of the core in m^2, and B_{max} is the maximum flux density in Gauss.

In the example:

I_{P_pk} = 1.23A, L_m = 899μH, EDR-28 core is chosen and its A_e = 88m^2.

Set B_{max} = 2950 Gauss. Obtain N_{P_min} > 42.5 turns.

Now all the parameters of transformer are determined, including N_{P_min}, N_P/N_S, N_S/N_A and L_m.

N_P = 43T, N_S = 43/2.62 = 16.4T, choose 16T, N_A = 16/2.35 = 6.8T, choose 7T.

Step 3. Current Sense Resistor Determination

Current sense resistor R_{CS} can be determined as the following equation:

$$R_{CS} = \frac{1}{2} \times \frac{N_P}{N_S} \times \frac{K_{CC}}{I_O} \times CTR_{TX1}$$

where K_{CC} is a reference in the controller.

In the example:

Actual N_P/N_S = 2.69, K_{CC} = 0.25, I_O = 0.4A, CTR_{TX1}= 0.9,

The current sense resistor R_{CS} will become (1/2)*2.69*(0.25/0.4)*0.9 = 0.79 Ω.

Step 4. Bridge Rectifier Determination

The maximum reverse voltage of the bridge rectifier V_{RRM_max} can be expressed as:

$$V_{RRM\_max} = \sqrt{2} \cdot V_{ac\_max}$$

The maximum forward current of the bridge rectifier I_{BR_max} can be expressed as:

$$I_{BR\_max} = \frac{P_{in\_max}}{V_{ac\_min}}$$

In the example:

$$V_{RRM\_max} = \sqrt{2} \cdot 264 = 373V$$

I_{BR_max} = 22.12/90 = 0.25A

A 600V / 1A diode bridge will provide sufficient de-rating, including inrush current and voltage surge.

Step 5. MOSFET Determination

The maximum drain-to-source voltage stress of the MOSFET V_{DS_max} is given as:

$$V_{DS\_max} = V_{RRM\_max} + V_{clamp}$$

in which V_{clamp} is the maximum voltage on the snubber and it must be higher than V_{ro}.

The maximum drain-to-source current stress of the MOSFET I_{DS_max} is given as:

$$I_{DS\_max} = \sqrt{2} \cdot V_{ac\_min} \cdot \frac{t_{on\_max}}{L_m}$$

In the example:

Set V_{clamp} = 160V

V_{DS_max} = 373+160 = 533V : for sufficient de-rating, choose at least 650V rated MOSFET.

$I_{DS\_max} = I_{P\_pk}$ = 1.23A : MOSFET R_{dson} selection depends on thermal aspects. In this small T8 design, a 4A MOSFET with R_{dson} of 1.8Ω was selected, which can be used without heat-sink.

Step 6. Output Diode and Auxiliary Diode Determination

The maximum reverse voltage stress of the output diode V_{Do_max} can be expressed as:

$$V_{Do\_max} = V_{RRM\_max} \cdot \frac{N_S}{N_P} + V_{o\_OVP}$$

where V_{O_OVP} is the output over voltage level.

The maximum average forward current stress of the output diode I_{Do_max} can be expressed as:

$$I_{Do\_max} = I_o$$

In the example:

Set V_{O_OVP} = 61V

V_{Do_max} = 373/2.62+61 = 203V

I_{Do_max} = I_O = 0.4A

Diodes with higher current rating can be chosen for higher efficiency.

The maximum reverse voltage stress of the auxiliary diode V_{Da_max} can be expressed as:

$$V_{Da\_max} = V_{RRM\_max} \cdot \frac{N_A}{N_P} + V_{DD\_OVP}$$

where V_{DD_OVP} is the VDD over voltage level.

The maximum average forward current stress of the output diode I_{Da_max} can be expressed as:

$$I_{Da\_max} = I_{DD\_max}$$

in which I_{DD_max} is the maximum supply current for the controller.

In the example:

V_{DD_OVP} = 27V

V_{Da_max} = 373/(2.62*2.35)+27 = 87.8V

I_{Da_max} = I_{DD_max} = 5mA

Step 7. Minimum On-Time Setting

RT7302 limits a minimum on-time t_{on_min} for each switching cycle. The t_{on_min} is a function of the sample-and-hold ZCD current I_{ZCD_SH} as following:

$$t_{on\_min} \cdot I_{ZCD\_SH} = 405\ p \cdot sec \cdot A\ (typ.)$$

I_{ZCD_SH} can be expressed as:

$$I_{ZCD\_SH} = \frac{V_{in} \cdot N_A}{R_{ZCD1} \cdot N_P}$$

Thus, R_{ZCD1} can be determined by:

$$R_{ZCD1} = \frac{t_{on\_min} \cdot V_{in}}{405p} \cdot \frac{N_A}{N_P} (typ.)$$

In addition, the current flowing out of ZCD pin must be lower than 2.5mA (typ.). Thus, the R_{ZCD1} is also determined by:

$$R_{ZCD1} > \frac{\sqrt{2} \cdot V_{ac\_max}}{2.5m} \cdot \frac{N_A}{N_P}$$

In the example:

$$R_{ZCD1} > \sqrt{2} * 264/2.5mA/(2.62*2.35) = 24.2k\Omega$$

Set R_{ZCD1} =60kΩ

When V_{in} = 10V, t_{on_min} = 405p*60k*(2.62*2.35)/10 = 14.9μs

In general, longer t_{on_min} can slightly improve THDi. However, if t_{on_min} is too long, it will induce a current resonance at V_{in} zero crossing, worsening THDi. Thus, t_{on_min} can be properly defined according to the measured THDi.

Step 8. Output Over-Voltage Protection Setting

Output OVP is achieved by sensing the knee voltage on the auxiliary winging. Thus, R_{ZCD1} and R_{ZCD2} can be determined by the equation as:

$$V_{O\_OVP} \cdot \frac{N_A}{N_S} \cdot \frac{R_{ZCD2}}{R_{ZCD1} + R_{ZCD2}} = 3.1V (typ.)$$

In the example:

Set V_{O_OVP} = 61V

It can be calculated that R_{ZCD2} =7.9kΩ

Step 9. Propagation Delay Compensation Design

The V_{CS} deviation (ΔV_{CS}) caused by propagation delay effect can be derived as:

$$\Delta V_{CS} = \frac{V_{in} \cdot t_d \cdot R_{CS}}{L_m},$$

in which t_d is the delay period which includes the propagation delay of RT7302 and the turn-off transition of the main MOSFET. The sourcing current from CS pin of RT7302 I_{CS} can be expressed as:

$$I_{CS} = K_{PC} \cdot V_{in} \cdot \frac{N_A}{N_P} \cdot \frac{1}{R_{ZCD1}}$$

where K_{PC} is a constant value in the controller. R_{PC} can be designed by:

$$R_{PC} = \frac{\Delta V_{CS}}{I_{CS}}$$

$$= \frac{t_d \cdot R_{CS} \cdot R_{ZCD1}}{L_m \cdot K_{PC}} \cdot \frac{N_P}{N_A}$$

t_d is estimated to be around 150ns

In the example:

R_{PC} = 150n*0.74*60k/(899µ*0.02)*(2.62*2.35) = 2.3kΩ

The delay period td is varied with the parasitic capacitance of MOSFET, the gate driving capability, and the propagation delay of the controller. Thus, t_d cannot be estimated accurately, and R_{PC} may need to be modified according to the measured output current. If the output current increases when V_{in} rises, R_{PC} should be increased. If the output current decreases with V_{in} rises, R_{PC} should be decreased.

Step 10. Feed-Forward Compensation Design (Only for RT7302)

The COMP voltage, V_{COMP}, can be derived from the following equations.

$$\frac{1}{2}\left(V_{MULT\_pk}\right)^2 \times \frac{t_{on} + t_{off}}{t_S} \times Gm_{ramp} \times t_{on} = C_{ramp} \times V_{COMP}$$

$$V_{MULT\_pk} = V_{in\_pk} \times \frac{R_{M2}}{R_{M1} + R_{M2}}$$

V_{MULT_pk} is the peak voltage on the MULT pin. Gm_{ramp} is the trans-conductance of the ramp generator, and its typical value is 2.5µA/V. C_{ramp} is the capacitance of the ramp generator, and its typical value is 6.5pF. When the converter operates at CRM, (t_{on} + t_{off}) / t_S=1. V_{COMP_min} is recommended be within 1.2 ~ 1.5V, and R_{M2} is recommended to be within 30 ~ 60kΩ. Thus, the voltage divider resistors R_{M1} and R_{M2} can be determined according to the above parameters.

In the example:

t_{on_max} = 8.68μs.

Set V_{COMP_min} = 1.2V,

Obtain V_{MULT_pk} = 0.85V.

Set R_{M2} = 43kΩ,

It can be calculated that R_{M1} = 6.4MΩ.

4. Design Tool Explanation

The RT7302 design tool and RT7304 design tool can be used as quick way to determine the component values. The content is similar to the step by step design as described in Chapter 3. In the design tool, users input operation parameters into "Yellow Grid". According to the key-in parameter, the design tool will automatically generate the results in Pink Grid".

Table 1 below shows the entered data and calculation results for the 18W T8 reference design.

Table 1. Design tool data

Step1: Input and output conditions Definition		
Min. AC input voltage V_{ac_min} =	90	Vrms
Max. AC input voltage V_{ac_max} =	264	Vrms
Line frequency f_{line} =	50	Hz
Average output current I_o =	0.4	A
Min. average output voltage V_{o_min} =	43.0	V
Max. average output voltage V_{o_max} =	47.0	V
Max. average output power P_{o_max} =	18.8	W
Estimated efficiency η =	85	%
Estimated peak current transfer ratio (CTR) of the transformer(TX_1) (I_{sec_pk} / I_{pri_pk})*(N_S / N_P) =	90	%
Estimated half of the resonant period of the primary-side inductance L_m and parasitic capacitance of MOSFET Q_1 =	1.00	µs
Estimated deviation of the detected inductance discharge time T_{OFF} =	0.50	µs
Estimated max. average input power $P_{in\_max\_est}$ =	22.12	W
Forward voltage of output diode V_f =	0.7	V
Max. voltage of "V_{o_max}*N_P/N_S" V_{FD} =	125	V
Min. VDD supply voltage at V_{o_max} $V_{DD\_Vomax\_min}$ =	14.2	V
VDD supply voltage at V_{o_max} V_{DD_max} =	20	V

Step2: Transformer (TX_1) Design		
1. Turns ratio determination		
Ideal turns ratio of primary to secondary windings N_P / N_S =	2.62	
Ideal turns ratio of secondary to auxiliary windings N_S / N_A =	2.35	
2. Inductance design		
The lowset switching frequency f_{s_min} =	54.00	kHz
Max. on time of the MOSFET t_{on_max} =	8.68	µs
Duty ratio at the peak of the min. AC input voltage D_{on_max} =	0.47	
Factor(t) at the min. AC input voltage Factor(t) $_{min}$ =	35.13	
Primary-side Inductance L_m =	898.87	uH
3. Current Stress Calculation (@min. AC input voltage and full load)		
Max. peak current of the primary winding I_{P_pk} =	1.229	A
RMS current of the primary winding I_{P_rms} =	0.369	A
Max. peak current of the secondary winding I_{S_pk} =	3.303	A
RMS current of the secondary winding I_{S_rms} =	0.912	A
4. Structure design		
Max. magnetic flux density B_{max} =	2950	Gauss
Cross sectional area of core A_e =	88	mm2
Min. turns number of the primary winding N_{P_min} >	42.56	Turns
Turns number of the primary winding N_P =	43	Turns
Turns number of the secondary winding N_S =	16	Turns
Turns number of the auxiliary winding N_A =	7	Turns
Actual N_P/N_S =	2.69	
Actual N_S/N_A =	2.29	
Current Density J =	8	A/mm2
Wire Diameter of the Primary Winding r_P ≥	0.24	mm
Selected Wire Diameter of the Primary Winding r_P =	0.27	mm
Current density of the primary winding J_{pri} =	6.452	A/mm²
Total wire Area of Primary Winding A_P =	2.46	mm²
Wire Diameter of the Secondary Winding r_S ≥	0.38	mm
Selected Wire Diameter of the Secondary Winding r_S =	0.3	mm
Current density of the secondary winding J_{sec} =	12.908	A/mm²
Total wire Area of the Secondary Winding A_S =	3.14	mm²
Selected Wire Diameter of the Auxiliary Winding r_A =	0.12	mm
Total Wire Area of the Auxiliary Winding A_A =	0.08	mm²
Selected Transformer A_W =	23.10	mm²
Transformer Fill Factor K_W =	0.246	

Step3: Current Sense Resistor(R_{CS}) Determination		
Ideal current sense resistor R_{CS} =	0.79	Ω
Selected current sense resistor R_{CS} =	0.74	Ω
Actual average output current I_o =	0.429	A
Max. CS peak voltage $V_{CS\_pk\_max}$ =	0.91	V
Ratio of the V_{CS_CL} to $V_{C\_pk\_max}$ V_{CS_CL} / $V_{CS\_pk\_max}$ =	1.02	

Step4: Bridge Rectifier(BD) Determination		
Max. reverse voltage of the bridge rectifierV_{RRM_max} =	373	V
Max. forward current of the bridge rectifier I_{BR_max} =	0.25	A

Step5: MOSFET(Q_1) Determination		
Max. voltage on the snubber V_{clamp} =	160.00	V
Max. D-to-S voltage stress of the MOSFET V_{DS_max} =	533.4	V
Max. D-to-S current stress of the MOSFET I_{DS_max} =	1.229	A

Step6: Output diode(D_{OUT}) and Auxiliary Diode(D_{AUX}) Determination		
Max. reverse voltage stress of the output diode V_{Do_max} =	200.0	V
Max. average forward current stress of the output diode I_{Do_max} =	0.400	A
Max. reverse voltage stress of the auxiliary diode V_{Da_max} =	87.8	V
Max. average forward current stress of the auxiliary diode I_{Da_max} =	5.000	mA

Step7: Min. on Time Design		
High-side resistor of the ZCD resistor-divider R_{ZCD1} >	24.31	kΩ
R_{ZCD1} =	60.00	kΩ
Min. on time @ V_{CSIN}=10V $t_{on(min)}$ =	14.93	µs

Step8: OVP Setting		
Ratio of the output OV to max. output voltages V_{o_ovp}/V_{o_max} =	1.30	
Output over-voltage threshold V_{o_ovp} =	61.10	V
Low-side resistor of the ZCD resistor-divider R_{ZCD2} =	7.87	kΩ

Step9: Propagation Delay Compensation Design		
IC Propagation delay+MOSFET turn off transition t_D =	150.00	ns
Propagation delay compensation resistor R_{PC} =	2.28	kΩ

Step10: Feed-Forward Compensation Design		
Recommedned Min. COMP voltage V_{COMP_min} =	1.20	V
Recommedned Min. MULT voltage V_{MULT_min} =	0.85	V
Low-side resistor of the MULT resistor-divider R_{M2} =	43	kΩ
High-side resistor of the MULT resistor-divider R_{M1} =	6.4	MΩ

Step11: Recommended Component Value		
High-voltage start-up resistor R_{HV} =	10 ~ 22	kΩ
External GATE-to-GND resistor R_{gs} =	10 ~ 22	kΩ
Gate resistor between GATE pin and MOSFET(Q_1) gate R_g =	10 ~ 100	Ω
Resistor in series with the diode(D_{AUX}) R_{Aux} =	10 ~ 100	Ω
Parallel resistor of the MOSFET snubber R_{Sn1} =	100 ~ 300	kΩ
Series resistor of the MOSFET snubber R_{Sn2} =	100 ~ 300	Ω
VDD decoupling capacitor C_{VDD} =	10 ~ 33	µF
Compensation capacitor between the COMP and GND pins C_{comp} =	1 ~ 4.7	µF
Filter capacitor between the MULT and GND pins C_{Mult} =	10 ~ 1000	pF (Dim
	1 ~ 100	nF (Nor
Filter capacitor between the ZCD and GND pins C_{ZCD} =	10 ~ 22	pF
Capacitor of the MOSFET snubber C_{Sn1} =	1 ~ 2.2	nF

5. Circuit Diagram of the Evaluation Board

The circuit diagram of the evaluation board is shown in Figure 4 below.

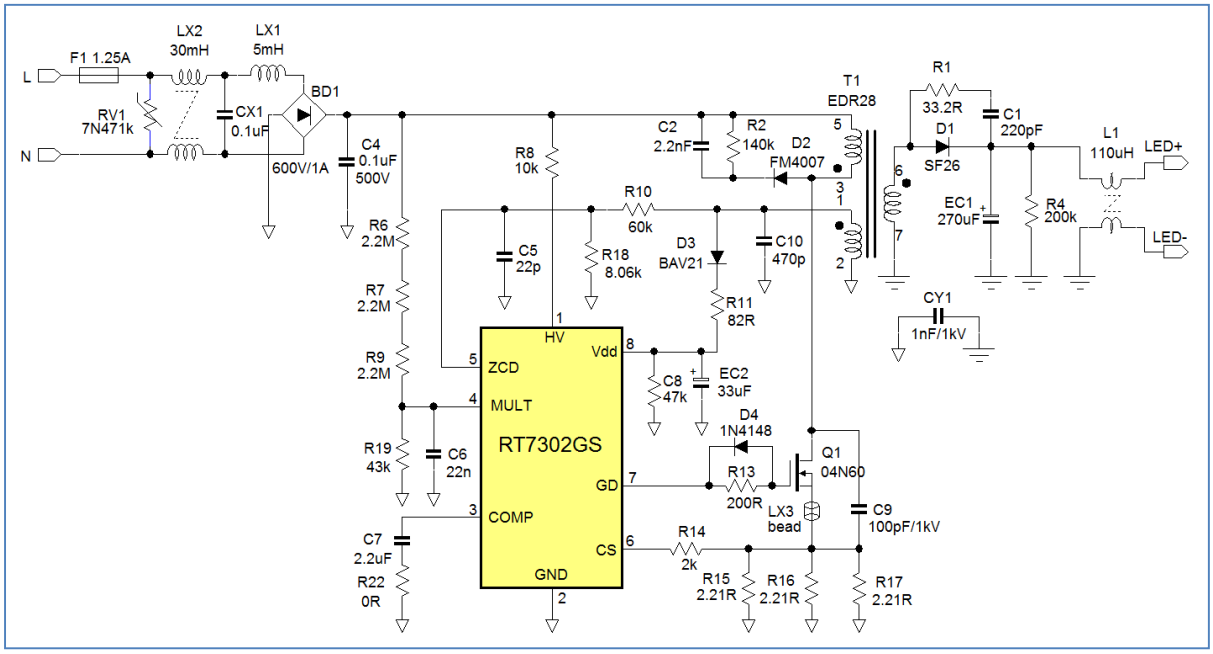


Figure 4. Schematic of the 18W T8 LED driver reference design

RV1 is added for line surge protection. LX2, CX1 and LX1 are added to reduce Line conducted EMI. L1 and LX3 are added to reduce radiated EMI.

The full BOM is shown in table 2 below.

Table 2. Full BOM of the 18W LED driver reference design

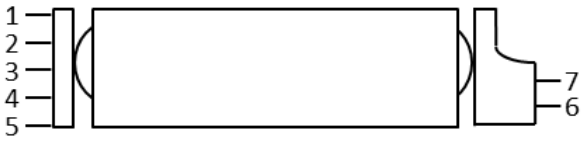
Item	Quantity	Reference	Part/Value	Type	Vendor	Remark
1	1	F1	T1.25A/300V	SS-5F-2P	Littlefuse	
2	1	RV1	7N471K	TVS-2P	Thinking	
3	1	LX2	30mH	LRS-T14	Abliss	T12.7*7.92*4.9(μi=10000)
4	1	CX1	0.1μF	CFS-12X12	Shiny Space	
5	1	LX1	5mH	LDS-D9X12	Mag. layers	
6	1	BD1	1A/600V	DB-1A	GW	
7	1	C4	0.1μF/500V	CFS-11X10	Murata	
8	3	R6, R7, R9	2.2MΩ	0805	RALEC	
9	1	R19	43kΩ	0603	RALEC	
10	1	C6	22nF/50V	0603	Murata	
11	1	C7	2.2μF/25V	0805	Murata	

12	1	R22	0Ω	0603	RALEC	
13	1	R8	10kΩ	1206	RALEC	
14	1	R2	140kΩ	1206	RALEC	
15	1	D2	FM4007	SOD123	Willas	
16	1	C2	2.2nF/1kV	1206	Murata	
17	1	R13	200Ω	0805	RALEC	
18	1	D4	1N4148	SOD-123	Willas	
19	1	Q1	4A/650V	TO-220	IPS	FTA04N65D
20	1	C9	100pF/1kV	1206	Murata	
21	1	LX3	T3.5*3*1.4	---	King core	On Source pin of Q1
22	3	R15, R16, R17	2.21Ω	1206	RALEC	
23	1	R14	2kΩ	603	RALEC	
24	1	C10	470pF/1kV	1206	Murata	
25	1	CY1	1000pF/250Vac	CAP-10mm	Murata	
26	1	R10	60kΩ	0603	RALEC	
27	1	R18	8.06kΩ	0603	RALEC	
28	1	C5	22pF	0603	Murata	
29	1	D3	BAV21	SOD-123	Willas	
30	1	R11	82Ω	0603	RALEC	
31	1	EC2	33μF/50V	CES-5X11	Rubycon	
32	1	T1	EDR28	EDR28	Abliss	
33	1	U1	RT7302	SOP-8	Richtek	
34	1	D1	SF26	DO-15	Willas	
35	1	R1	33Ω	1206	RALEC	
36	1	C1	220pF/1kV	1206	Murata	
37	1	EC1	270μF/63V	CES-10X25	Rubycon	
38	1	L1	110μH	LR-T9	Abliss	T9*5*3(μi=10000)
39	1	R4	200kΩ	1206	RALEC	

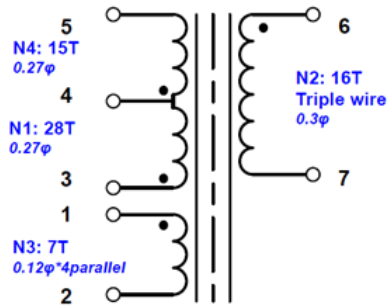
Transformer design: The transformer design specification is shown in Figure 5.

Transformer Specification

Core Size:	EDR-28
Material:	PC40
Bobbin/PINs:	Horizontal / 7pins
Primary inductor: (± 5%)	920μH
Leakage inductor:	30μH



Electrical:



Winding Specifications:

Winding No.	PIN	Wire	Turns	Winding Type	Tape Layer
N1	3 → 4	0.27φ	28Ts	Close winding	2 Layers
N2	6 → 7	Triple wire 0.3φ	16Ts	Close winding	2 Layers
N3	1 → 2	0.12φ x 4 parallel	7Ts	Close winding	1 Layer
N4	4 → 5	0.27φ	15T	Close winding	1 Layer

Figure 5. Transformer specification

The primary side formed by sandwich structure is used to reduce the leakage inductance of the transformer, improving the efficiency and the output current regulation. To improve radiation EMI, the maximum voltage swing which is on pin 3 of the transformer, should be at the most inner side. To meet the safety standard, Triple wire at the secondary side is normally adopted for providing insulation.

6. Electrical Performance Measurements

Table 3 below shows the LED driver input and output parameters over the full mains voltage range.

Table 3. Performance measurements

Frequency	Vac [V]	Pin [Watt]	Vout [V]	Iout [mA]	Pout [Watt]	Eff. [%]	PF Value	THD
60Hz	90	21.54	45.75	405	18.53	86.02%	0.9960	6.37
60Hz	100	21.24	45.78	405	18.54	87.29%	0.9960	6.68
60Hz	110	21.03	45.80	404	18.50	87.98%	0.9954	7.03
60Hz	120	20.87	45.83	403	18.47	88.50%	0.9950	7.24
60Hz	132	20.73	45.86	402	18.44	88.93%	0.9944	7.53
50Hz	180	20.60	46.00	401	18.45	89.54%	0.9908	7.51
50Hz	200	20.60	46.07	400	18.43	89.46%	0.9886	7.02
50Hz	220	20.64	46.15	400	18.46	89.44%	0.9851	6.73
50Hz	230	20.69	46.23	400	18.49	89.38%	0.9832	6.82
50Hz	240	20.75	46.31	400	18.52	89.27%	0.9811	6.99
50Hz	264	20.90	46.44	400	18.58	88.88%	0.9738	7.86

Current regulation = 1.23%

ΔEfficiency = 3.52%

Maximum PF = 0.996

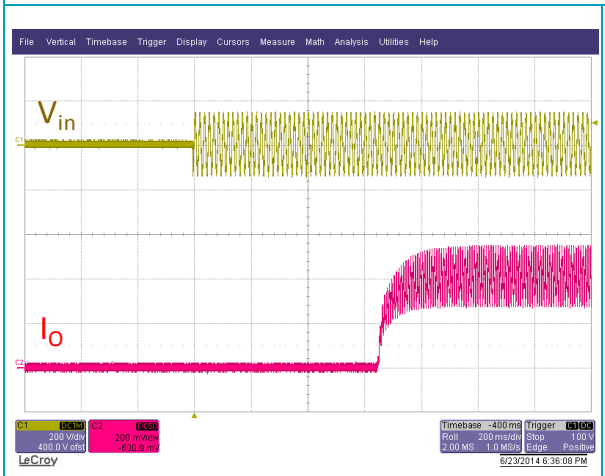
Minimum PF = 0.974

As can be seen, the current line regulation is excellent. Driver efficiency meets the target easily, and Power Factor and THDi are fully in line with regulations for lighting applications.

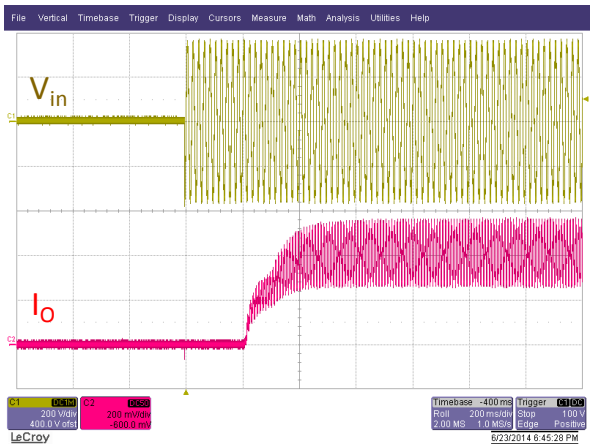
The figures in Table 4 show voltage and current waveforms during various operation conditions:

Table 4. Measured waveforms during various operation conditions

Start-up

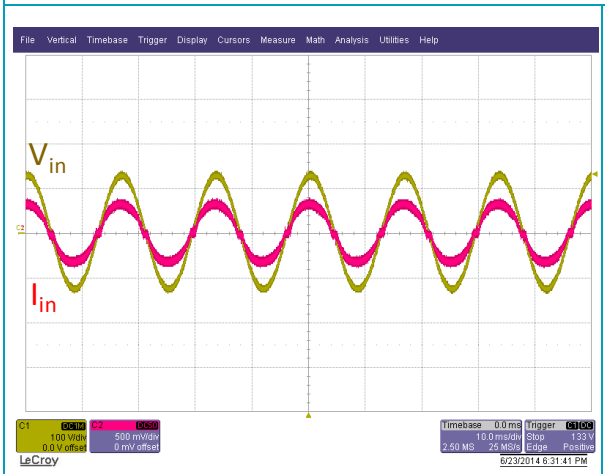


Vin = 90Vac: T-start = 630msec

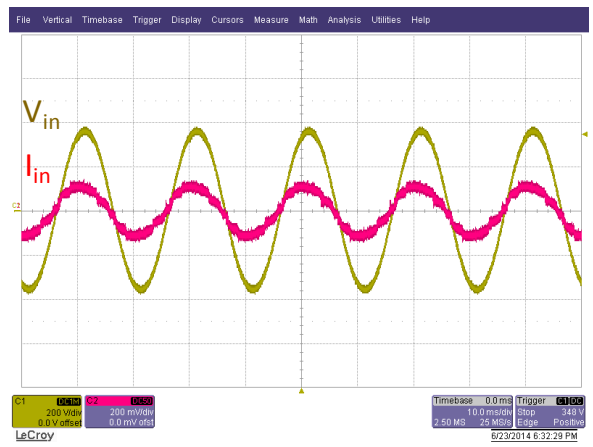


Vin = 264Vac: T-start = 210msec

Input waveform



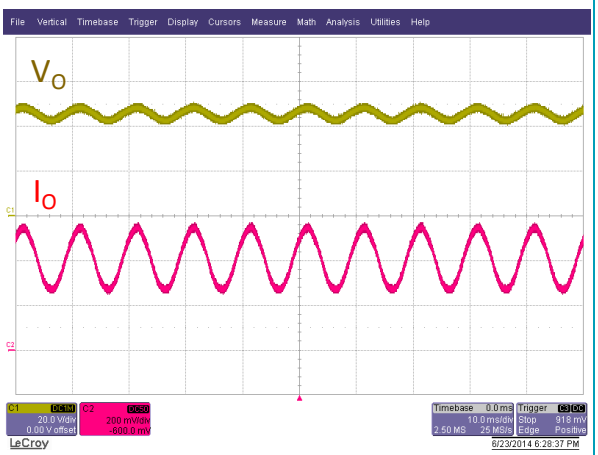
Vin = 90Vac



Vin = 264Vac

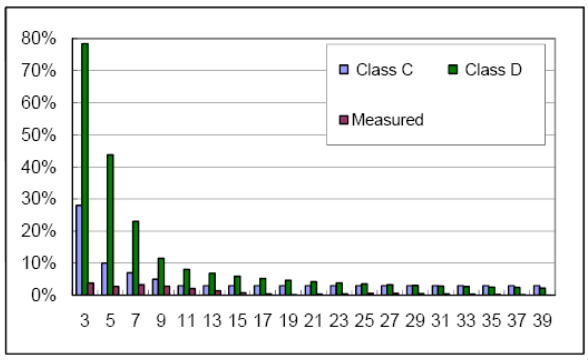
Output waveform

Vin = 90Vac

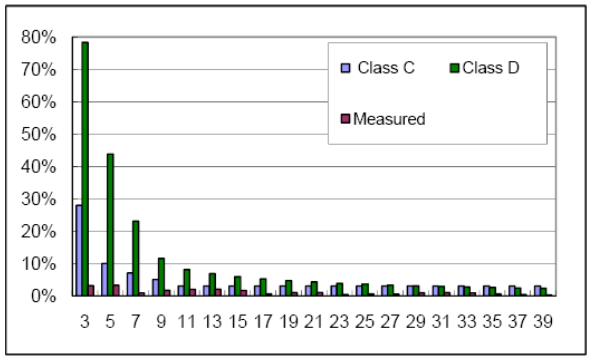


Vin = 264Vac

Harmonic content of input current: (IEC61000-3-2)

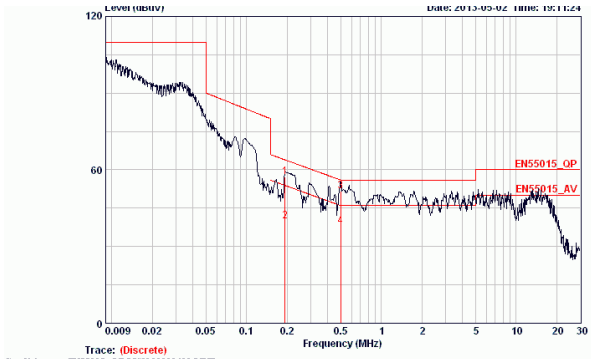


Vin = 110Vac: passes Class C and D

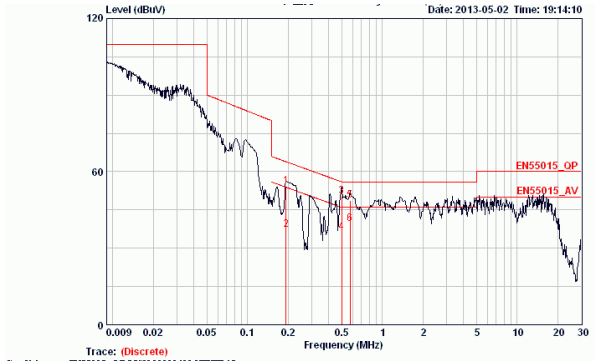


Vin = 230Vac: passes Class C and D

Conduction EMI



Vin = 230V-L



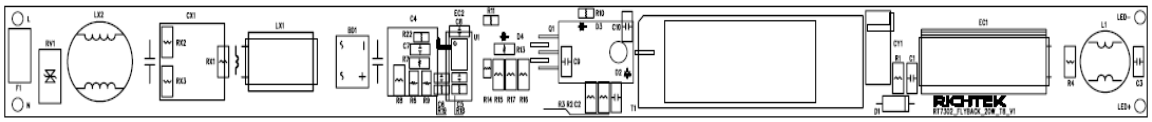
Vin = 230V-N

The demo board passes conducted and radiated EMI at 120V and 230Vac

7. PCB Layout Information

The PCB layout of the reference design is shown in Figure 6 below. It is build from double-sided FR-4 material and uses a narrow form-factor to make it suitable to fit into narrow T8 enclosures.

To minimize EMI, current loops of the gate drive, snubber circuit, output diode and main MOSFET switching loop should be kept as small as possible. Ground of the IC, sense resistor, aux winding and Y-capacitor should all go to one central ground point on the input capacitor ground. Capacitors on the IC COMP pin, ZCD pin and MULT pin should be as close as possible to the IC.



Top silk (Component location)

Top trace

Bottom trace

Figure 6. PCB Layout

8. Summary

With the help of this step by step design guide and the RT7302 design tool, the user is able to quickly design a LED driver that fulfills the requirements for high performance offline LED drivers. The absence of secondary side sensing greatly simplifies the mechanical design, and allows small form-factor PCB design.

When all guidelines are followed, the design should fulfill EMI and pass the surge tests. Although this reference design is for an 18W LED driver, RT7302 can be used in a wide range of LED driver designs, ranging from 8W ~ 60W.

Related Parts		
RT7302	Primary-Side-Regulation Dimmable LED Driver Controller with Active PFC	Datasheet
RT7304	Primary-Side-Regulation Dimmable LED Driver Controller with Active PFC	Datasheet

Next Steps	
Richtek Newsletter	Subscribe Richtek Newsletter
Download	Download PDF
Application	LED Lighting

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: 886-3-5526789